



DO-214AA SMB Package Thyristor Surge Suppressors TSS P0080SB VDRM 6V VS 25V

Basic Information

- Place of Origin: Shenzhen, Guangdong, China
- Brand Name: SOCAY
- Certification: REACH,RoHS,ISO
- Model Number: P0080SB
- Minimum Order Quantity: 2500PCS
- Price: Negotiable
- Packaging Details: AMMO packing bulk
- Delivery Time: 5-8 work days



Product Specification

- Description: Thyristor Surge Suppressors (TSS)
- Package Type: DO-214AA/SMB
- VDRM (Min.): 6V
- IDRM: 5 μ A
- Vs @100V/ μ S (Max.): 25V
- Is (Max.): 800mA
- Vt @It=2.2A (Max.): 4V
- It (Max.): 2.2A
- Ih (Min.): 50mA
- C0 @1MHz,2V Bias (Typ.): 80pF
- Highlight: **SMB Thyristor Surge Suppressors ,
DO-214AA Thyristor Surge Suppressors ,
P0080SB**

Product Description

(TSS) P0080SB DO-214AA (SMB) Package Thyristor Surge Suppressors VDRM 6V VS 25V Marking P008B

DATASHEET: [PXXX0SB_v2103.1.pdf](#)

Part Number	Marking	V _{DRM} @I _{DRM} =5 μA	V _S @100V/μ S	V _T @I _T =2.2 A	I _S	I _T	I _H	C0 @1MHz, 2V bias
		V min	V max	V max	mA max	A max	mA min	pF typ
P0080SB	P008B	6	25	4	800	2.2	50	80
P0300SB	P03B	25	40	4	800	2.2	50	80
P0640SB	P06B	58	77	4	800	2.2	150	80
P0720SB	P07B	65	88	4	800	2.2	150	75
P0900SB	P09B	75	98	4	800	2.2	150	70
P1100SB	P11B	90	130	4	800	2.2	150	70
P1300SB	P13B	120	160	4	800	2.2	150	65
P1500SB	P15B	140	180	4	800	2.2	150	65
P1800SB	P18B	170	220	4	800	2.2	150	65
P2300SB	P23B	190	260	4	800	2.2	150	60
P2600SB	P26B	220	300	4	800	2.2	150	60
P3100SB	P31B	275	350	4	800	2.2	150	50
P3500SB	P35B	320	400	4	800	2.2	150	50
P4200SB	P42B	400	520	4	800	2.2	150	40

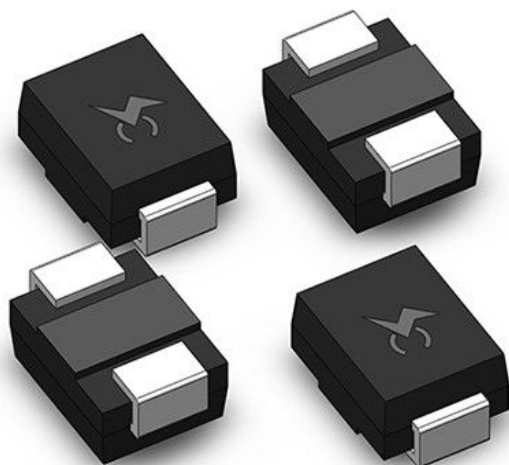
Notes:

V_S is measured at 100KV/s.

Off-state capacitance is measured in V_{DC}=2V, V_{RMS}=1V, f=1MHz.

About TSS

The TSS are characterised by precise conduction, fast response, high surge absorption capacity, biaxial symmetry and high reliability.



Description:

PXXX0SB Series are designed to protect broadband equipment such as modems, line card, CPE and DSL from damaging over-voltage transients. The series provides a surface mount solution that enables equipment to comply with global regulatory standards.

Features:

- u Low voltage overshoot
- u Low on-state voltage
- u Does not degrade surge capability after multiple surge events within limit
- u Fails short circuit when surged in excess of ratings
- u Low Capacitance

Parameter	Definition
I_S	Switching Current - maximum current required to switch to on state
I_{DRM}	Leakage Current - maximum peak off-state current measured at V_{DRM}
I_H	Holding Current - minimum current required to maintain on state
I_T	On-state Current - maximum rated continuous on-state current
V_S	Switching Voltage - maximum voltage prior to switching to on state
V_{DRM}	Peak Off-state Voltage - maximum voltage that can be applied while maintaining off state
V_T	On-state Voltage - maximum voltage measured at rated on-state current
C_0	Off-state Capacitance - typical capacitance measured in off state

Series	2/10 μ S ¹	8/20 μ S ¹	10/160 μ S ¹	10/560 μ S ¹	10/1000 μ S ¹	5/310 μ S ¹	I_{TSM} 50/60 Hz	di/dt
	2/10 μ S ²	1.2/50 μ S ²	10/160 μ S ²	10/560 μ S ²	10/1000 μ S ²	10/700 μ S ²		
	A min	A min	A min	A min	A min	A min	A min	Amps/ μ S max
B	250	250	150	100	80	100	30	500

Notes: Current waveform in μs Voltage waveform in μs	- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product. - I_{PP} ratings applicable over temperature range of -40°C to $+85^{\circ}\text{C}$ - The device must initially be in thermal equilibrium with $-40^{\circ}\text{C} < T_J < +150^{\circ}\text{C}$
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High Temp Voltage Blocking	80% Rated VDRM (VAC Peak) $+125^{\circ}\text{C}$ or $+150^{\circ}\text{C}$, Lead Material Copper Alloy High Temp Voltage Blocking 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101	
Temp Cycling	-65°C to $+150^{\circ}\text{C}$, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104	
Biased Temp & Humidity	52 VDC ($+85^{\circ}\text{C}$) 85%RH, 504 up to 1008 hrs. EIA/ JEDEC, JESD22-A-101	
High Temp Storage	$+150^{\circ}\text{C}$ 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101	
Low Temp Storage	-65°C , 1008 hrs.	
Thermal Shock	0°C to $+100^{\circ}\text{C}$, 5 min. dwell, 10 sec. transfer, Thermal Shock 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106	
Autoclave (Pressure Cooker Test)	$+121^{\circ}\text{C}$, 100%RH, 2atm, 24 up to 168 hrs. EIA/Cooker Test) JEDEC, JESD22-A-102	
Resistance to Solder Heat	$+260^{\circ}\text{C}$, 30 secs. MIL-STD-750 (Method 2031)	
Moisture Sensitivity Level	85%RH, $+85^{\circ}\text{C}$, 168 hrs., 3 reflow cycles Level ($+260^{\circ}\text{C}$ Peak). JEDEC-J-STD-020, Level 1	

Lead Material	Copper Alloy	
Terminal Finish	100% Matte-Tin Plated	
Body Material	UL recognized epoxy meeting flammability classification 94V-0	

Part Number	Component Package	Quantity	Packaging Option	Packaging Specification
Pxxx0SB	DO-214AA	2500	Tape & Reel - 12mm/13"tape	EIA -481 - D

Thermal Considerations				
Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	- 40 to + 150	$^{\circ}\text{C}$
	T_S	Storage Temperature Range	- 40 to +150	$^{\circ}\text{C}$
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	$^{\circ}\text{C/W}$

Figure 1 - V-I Characteristics

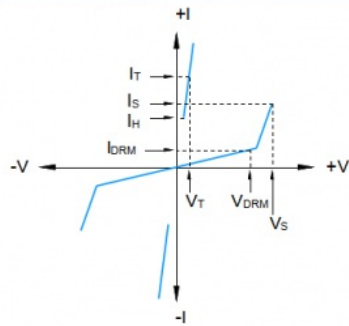
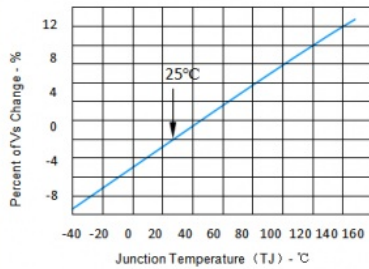
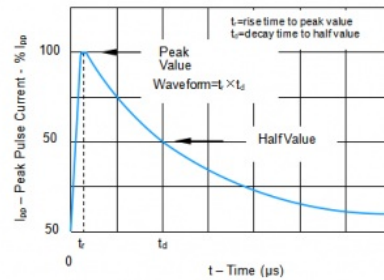
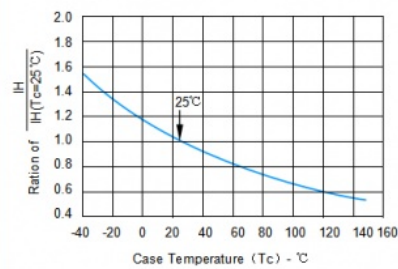
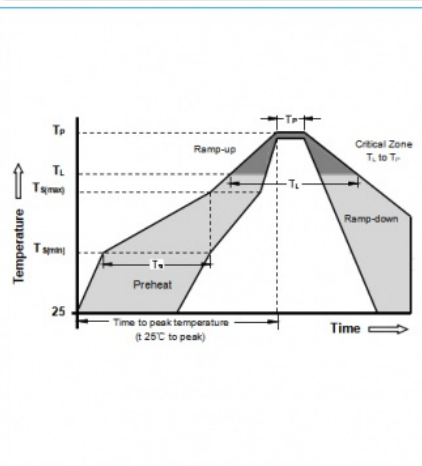
Figure 3 - Normalized V_S Change Versus Junction TemperatureFigure 2 - $t_r \times t_d$ Pulse Waveform

Figure 4 - Normalized DC Holding Current Versus Case Temperature



Soldering Parameters



Reflow Condition		Lead-free assembly
Pre Heat	-Temperature Min (T_{qmin})	+150°C
	-Temperature Max (T_{qmax})	+200°C
	-Time (min to max) (T_q)	60 - 180 Seconds
Average ramp up rate (Liquidus Temp T_L) to peak		3°C/Second Max
T_{Smax} to T_L - Ramp-up Rate		3°C/Second Max
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Time (min to max) (T_L)	60 - 150 Seconds
Peak Temperature (T_P)		260 +0/-5°C
Time within 5°C of actual peak Temperature (t_p)		30 Seconds Max
Ramp-down Rate		6°C/Second Max
Time 25°C to peak Temperature (T_P)		8 minutes Max
Do not exceed		+260°C

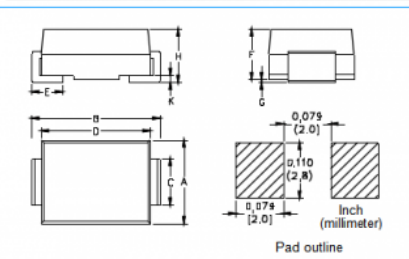
Part Numbering

Type	PXXX 0 S B
Median Voltage	
Construction Variable, 0: One chip	
2: Two chip	
E: ESD Protection	
Ipp Rating:	A @10/700 μs 2KV (50A) B @10/700 μs 4KV (100A) C @10/700 μs 6KV (150A) D @10/700 μs 8KV (200A)
Package Type S:	DO-214AA(SMB) T: DO-214AC(SMA) E: TO-92 L: DO-15, DO-27, DO-41 Y: SMB-H

Part Marking

PXXB	Part Marking Code (Refer to Electrical Characteristics Table)
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Dimensions DO-214AA



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.76	1.60
F	0.076	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41

Selection of semiconductor discharge tubes:

When selecting TSS, the following principles should generally be followed:

1. Selection of cut-off voltage VDRM: The cut-off voltage must be greater than the maximum operating voltage of the protected circuit;
2. Selection of transition voltage VBO: The transition voltage must be less than the maximum transient peak voltage that the

equipment can withstand;

3. Selection of the holding current I_H : the holding current must be greater than the operating current and short-circuit current of the equipment;

4. Selection of parasitic capacitance C : The parasitic capacitance is selected according to the insertion loss allowed by the circuit or the frequency of signal transmission;

5. Selection of surge current: Different levels of surge current are selected according to the requirements of the circuit or surge test standards.



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